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WE R&D.

RISC-V SoC Reference Architecture

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Automotive | RISC-V | FPGA

Confidential

This is an ongoing project under strict confidentially, so we can only share a very high level overview.

RISC-V is a free and open-source instruction set architecture (ISA) that seems to inspire the imagination and innovation of players in the semiconductor business. Technologically, it is not a leap forward compared to the incumbents, except for having a strong focus on modularity and extensibility in the design. In combination with the open standard approach of the project however, this creates an exiting new way of building SoCs.

The benefits of the design freedom however comes with the drawback of ecosystem fragmentation, compatibility and portability.

To manage this, we are supporting our customer in the design of a reference architecture, which should stand as focal point for developing tools and methods to deal with this issue.

FPGAs, Tools & IPs used in this project:

- [x] Genesys 2 AMD Kintex™ 7
- [x] Synopsys commercial RISC-V CPU - ARC-V
- [x] Synopsys commercial peripherals IPs
- [x] RISC-V CVA6 CPU
- [x] Segger debuggers
- [x] Open Source IP modules: UART, SPI, I2C, DRAM, AXI and Wishbone